CSC EMU Muon Sorter (MS)

Status
Plans

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Overview

• Functionality
  - Data formats
  - VME/JTAG interface
  - FPGA mezzanine
  - Firmware

• Tests done up to date
  - Standalone tests
  - Latency
  - SP-to-MS test
  - Beam test

• Plans for production and future tests
CSC EMU/Trigger Electronics
One board for both endcaps, resides in the middle of the Track Finder crate
Receives up to 3 LCTs from each of 12 Sector Processors over custom backplane
Does sorting “4 best out of 36” muons based on 7-bit “Quality” pattern
Transmits 4 best muons in ranked order to GMT over LVDS cables
### SP – to – MS Data Format

| Frame | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|    |
| 1 SE | BC0| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI| ETA| PHI|    |
| 2 SP | BX0| HL | C  | VC | RANK| HL | C  | VC | RANK| HL | C  | VC | RANK| HL | C  | VC | RANK| HL | C  | VC | RANK| HL | C  | VC | RANK| HL | C  | VC | RANK|    |

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<th>Synch</th>
<th>MUON 3</th>
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Here:
- **RANK** ................. PT LUT output, 5 bits PT and 2 bits Quality
- **ETA** ................. Pseudorapidity
- **PHI** .................. Azimuth coordinates
- **VC** .................... Valid Charge - 8th bit of PT LUT output
- **HL** .................... Halo muon trigger
- **C** ..................... Charge or muon sign
- **BX0** .................. The least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563).
- **BC0** .................. The Bunch Crossing Zero flag marks bunch zero data.
- **Synch** ............... Synchronization and spare bits
- **SE** ................... Synchronization error (data out of synch)
- **SP** ................... Spare bit

- **32-bit** GTLP point-to-point links from each SP
- **Data is transmitted in two frames at 80Mhz**
Has been agreed with the GMT Group

SCSI-3 68-pin AMP/Tyco 787171-5 connectors

Texas Instruments SN75LVDT386/LVDS387 receiver/driver chipset

Halogen-free cables, 9m estimated length for the CSC Track Finder
Muon Sorter Mezzanine and Main Boards

- Xilinx XC18V04 EPROMs
- Xilinx XC2V4000-FF1152 FPGA
• 12 links from Sector Processors, 12x32=384 inputs @ 80Mhz
• 4 links to LVDS transmitters, 4x32=128 outputs @ 80Mhz
• 1 status link (“winners”) back to SP’s, 24 outputs @ 80Mhz
• VME and CCB interfaces, ~80 inputs and outputs
• Input, intermediate and output FIFO buffers for testing purposes
LUT Conversion

Rank[6..0]          Pt_GMT[4..0]
                  |                  Quality_GMT[2..0]
                   ‘0’                     ‘0’
                   ‘0’
Phi_SP[4..0]        Phi_GMT[7..0]
SP_ID[3..0]         LUT 512x8
                     D[7..0]          D[4..0]
Eta_SP[4..0]        Eta_GMT[5..0]
SP_ID[3..0]

1 muon out of 4
Current Status and Future Tests

• 4 boards were built in 2003, 3 boards are completely assembled

• Have 2 mezzanines assembled (both FPGA are free donation from Xilinx)

• Two MS boards with mezzanines have been tested on the bench (next slide)

• Have been tested with Sector Processor prototype (next slide)

• Have been checked in the Track Finder crate during beam test at CERN in June 2004 (next slide)

• Do not require irradiation test
Standalone Tests of MS

- Need Track Finder crate, CCB, VME controller

- What was checked
  - Sorting Logic
  - LUT RAM’s
  - FIFO’s
  - Interface to GMT
  - VME/JTAG interface

- Load test patterns into FIFO_A, run them at 80Mhz through the sorter, check result from FIFO_B, FIFO_C, FIFO_D
  - >2M iterations without errors
VME/JTAG Interface

Xilinx XC2V4000 mezzanine FPGA and associated EPROM’s may be loaded/programmed from:

- Xilinx Parallel Cable IV
- Fairchild SCANPSC100F JTAG controller under VME control

National Semiconductor provides a free software to operate SCANPSC100F controller, that was adopted by UF to work via VME using SBS 620 Master.

- We have successfully run this software to program 4 EPROM’s residing on the mezzanine card
- Program time is ~1 min (~4 min over Xilinx Parallel Cable IV)
MS Latency

150 ns
Latency (2)

LVTTTL-GTLP-LVTTTL + backplane delay

LVTTTL-LVDS-LVTTTL + 1 m SCSI cable
• Load random test patterns into test FIFO (Test Point 3)
• Send @ 80Mhz to Muon Sorter
• Check data from FIFO_B and FIFO_C on MS board
• Check data from spy FIFO after Pt LUT on SP board
• Check winner bits from MS spy FIFO on SP board

>1M iterations without errors
Beam Test at CERN, June 2004

- Muon Sorter was receiving muons from 1 (2) Sector Processors during structured beam

- “Winner” bits were recorded by SP

- Run 380: ~12K events with 1 muon, 20 events with 2 muons, no events with 3 muons. One ambiguous event.

More details at http://www.phys.ufl.edu/~acosta/tb/talks/csctb04_sp_results.pdf
Cost Estimate

MS main board
• Components ............................................................... < $1000
• Services (PCB & front panel fabrication, assembly) ........ < $1000

Mezzanine card
• Components and services (FPGA, assembly) .............. $2500
Production and Testing Plans

• Design documentation is available on the web at http://bonner-ntserver.rice.edu/cms/projects.html#ms, including
  - specification
  - schematics
  - configuration file for EPROMs

• Need more tests with at least 2 SP and/or 12 Muon Tester cards (until December of 2004)

• Need to test with the GMT receiver card (never been done before). This fall or early next year?

• Plan to complete all tests by summer 2005.

• Based on results, we should decide if the final PCB should be built (currently have 5-6 minor PCB fixes).