CSC EMU/Track Finder
Clock and Control Board (CCB’2004)

Status
Plans

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Overview

• **Functionality**
  - Modes of operation
    “Discrete logic” mode
    “FPGA” mode and firmware
  - TTCrq mezzanine card
  - Clock distribution
  - Command distribution and decoding

• **Current status and tests done up to date**
  - Standalone tests
  - Test in the peripheral crate
  - Beam test
  - Irradiation test

• **Plans for CCB production and testing**
  - Cost estimate
  - Schedule
Muon Port Card (1)  
Clock Control Board  
Muon Sorter (1)  
Sector Processor (12)  
CSC Track-Finder Crate (1)  
In underground counting room  
On the periphery of the return yoke  
3 optical links  
On detector  
Trigger Motherboard (9)  
DAQ Motherboard (9)  
CSC Peripheral Crate (60)  
On detector  

CSC EMU/Trigger Electronics
Functionality

- Interface between the TTC system and CSC EMU/Track Finder Electronics

- Houses the TTCrq mezzanine card with TTCrx and QPLL ASICs

- Distributes 40/80Mhz clocks, Hard resets, broadcast and individual commands to custom EMU/TF backplanes

- May emulate TTC signals to peripheral and TF boards under VME control
Modes of Operation

• “Discrete Logic” Mode
  - TTCrq parallel outputs are latched/buffered only before distribution to custom backplane

  Expect to be the main operational mode at LHC

• “FPGA” Mode
  - TTCrq parallel outputs are passed through the Xilinx FPGA and may be processed there (for example, L1A can be delayed for a number of bunch crossings…). Useful for standalone and beam tests.
Discrete Logic Functions

- Performs basic VME A24D16 Slave functions
- Distributes 40Mhz and 80Mhz clocks to peripheral/TF backplane
- Translates the TTCrq parallel outputs onto GTLP backplane lines with intermediate registers/buffers
- Generates 500 ns Hard_Resets pulses for ALCT, DMB, TMB and CCB itself (FPGA) on broadcast or individual reset commands
- Monitors Conf_Done signals from all peripheral/TF boards
- Provides accesses to TTCrq mezzanine over serial I²C bus and to FPGA and EPROM over JTAG bus. All these operations are under VME control.
FPGA and Firmware

• One Xilinx XC2V250 FPGA
  $90 per chip
  Requires one XC18V02 EPROM
  Can be reloaded from EPROM on Hard_Reset (common and CCB-specific)
  FPGA reconfiguration time from EPROM is ~60 ms
  EPROM itself can be reprogrammed over Xilinx JTAG parallel cable or VME

• Existing firmware for the FPGA:
  - maintains the same functionality as discrete logic interface
  - provides more functional flexibility including:
    L1A generation (front panel, backplane, VME…) and programmable delays
    Able to generate all backplane signals (including reserved for future use)
    under VME control
    Read back unique board ID
New TTCrq Mezzanine Board

- TTCrx ASIC on the top side of the PCB
- QPLL radiation hard ASIC
- Additional 26-pin connector
  - 40Mhz clock LVDS output
  - 80(60) Mhz clock LVDS output
  - 160(120) Mhz clock LVDS output
  - control inputs/outputs
- Two 50-pin connectors backward compatible with the old TTCrm

- Preserves the functionality of the old TTCrm mezzanine
- Contains a quartz based phase-locked loop ASIC that outputs three clean clocks of 40, 80(60) and 160(120) MHz
  output jitter <50 ps peak-to-peak
- Reduced board height to comply with the VME mechanics
- Supported by EP-ESS group at CERN

http://ess.web.cern.ch/ESS/TTCsupport/
Clock Distribution

- **CCB’2004 has three sources of 40.08 Mhz clock:**
  - Clock40Des1 from TTCrx
  - Clock40 from QPLL
  - Clock40 from on-board oscillator

  One of these sources must be selected for a backplane distribution with a jumper (not programmable)

- **CCB’2004 has two sources of 80.16Mhz clock for the MPC:**
  - Clock80 from QPLL
  - Clock80 from on-board oscillator

  One of these sources must be selected for a backplane distribution with a jumper (not programmable)

- 40Mhz and 80Mhz clocks do not pass through the FPGA before routing to backplane in any mode

- All clocks are distributed over point-to-point LVDS lines on custom peripheral and Track Finder backplanes
Command Distribution and Decoding

• The CCB distributes over custom backplane:
  - Cmd[5..0]+BCntRes+EvCntRes + Cmd_Strobe for broadcast commands
  - Data[7..0] + Data_Strobe for individual commands
  - Hard Reset 500 ns pulses (individually for TMB, DMB, MPC, SP, MS)
  - several other status/special purpose signals

• It has been agreed that the only dedicated pulses distributed by CCB are the Hard Resets. All other signals (BC0, BC Reset…) should be decoded by TMB/DMB/MPC/SP/MS from the 6-bit command bus for broadcast commands and 6-bit data bus for individual commands.
Assembled Board

- Power consumption  
  - +5V: < 1A  
  - +3.3V: < 1A  
  - +1.5V: < 50 mA
Current Status and Tests

• 6 boards were built in spring of 2004, all equipped with the TTCrq mezzanines (2 at CERN, 1 at OSU, 3 at Rice)

• Have been tested on the bench (next slides)

• Have been tested with (almost) fully loaded peripheral crate (next slides)

• Have been checked in the peripheral crates at the beam test at CERN in June 2004 (next slides)

• Have been tested under irradiation at UC Davis cyclotron (next slides)
Standalone CCB’2004 Tests at Rice

• Have built a simple Tester Board to test the CCB, MPC, MS

• Have TTCvi/TTCvx board set with the 40.078Mhz clock source

• Have two 9U VME Wiener crates with peripheral and TF backplanes installed

• Have developed testing software to test the CCB’2004 with and without TTCvi/vx set in various modes

  Potential problem with one of 6 new TTCrq mezzanines (B channel) after power cycling. Will send to CERN for diagnostic/repair.
• Have checked the CCB’2004 at Rice in the peripheral crate with 7 DMB, 7 TMB and MPC (slots 2-5 in our crate are allocated for 6U boards only and can not be used for 9U cards)

• All clocks are point-to-point LVDS from the CCB to every slot in the crate. Broadcast command lines and command strobe are bussed GTLP lines.

• Quality of the GTLP strobe is acceptable with 15 target boards loaded. Variation in delay of the command strobe in respect to 40Mhz clock with 15 loads is < 3 ns. See various waveforms at http://bonner-ntserver.rice.edu/cms/pb_signals.ppt
• During unstructured beam the CCB’2004 was tested in “FPGA” mode with 9 target boards (4DMB + 4TMB + MPC) in the peripheral crate

• During structured beam two CCB’2004 were tested in “Discrete Logic” mode with 5 target boards each (2DMB + 2TMB + MPC)

• What was checked
  - TTCrq, VME and custom backplane interfaces
  - Both modes of operation
    40.08 and 80.16 Mhz clock distribution to target boards
    Broadcast command distribution (4 different commands)
• TTCrx and QPLL ASIC’s are built on radiation hard DMILL technology, see http://doc.cern.ch/yellowrep/2000/2000-010/p226.pdf

• Discrete CMOS logic that performs the basic functions of the CCB is radiation tolerant to expected dose (subject to test, next slide)

• FPGA may experience SEU, but can be reloaded periodically from its EPROM on Hard_Reset command the same way as other peripheral boards
  
  Same Xilinx Virtex-2 family as on DMB and TMB (but smaller FPGA)
Irradiation Test of the CCB’2004

Conducted in August 2004 at UC Davis 63 MeV cyclotron

Distribute TTC broadcast commands and L1Accepts from TTCvi/vx
Pass them through the CCB to peripheral backplane
Irradiate the discrete logic part of the board and the FPGA and EPROM
Monitor response to TTC commands and count L1A on a tester board
All boards under VME control, residing in one 9U crate (CCB on an extender)
Results of the Irradiation Test

- **CMOS discrete logic (registers, buffers, gates etc) irradiated up to 5 kRad**
  - No errors

- **Xilinx XC18V02 EPROM irradiated up to 5 kRad**
  - Was continuously read back over JTAG during irradiation, no errors

- **Xilinx XC2V250-4FG456 FPGA irradiated up to 5 kRad**
  - Observed SEU at 2.1 kRad, 2.9 kRad, 3.2 kRad
  - Recoverable after Hard reset
Production and Testing Plans

• Need to make ~10 minor changes in schematic/layout. Do not expect to add or remove any active components on board.

• Design documentation (specification, schematics, configuration file for EPROM) is available on the web at http://bonner-ntserver.rice.edu/cms/projects.html#ccb

• 70 boards will have to be built and assembled (including 15% spare)
  - will order ~5% more components for future repairs
  - TTCrq mezzanines have been ordered from CERN, expect by December

• In-house testing (Matveev, Lee, Tumanov)
  - need just a short chain (TTCvi/vx+CCB+MT) to test the functionality
  - may use small 9U crate and run a program similar to irradiation test
  - need to enhance this program including convenient GUI

• Burn in 24 hours at 60..70 C then test again (intend to use OSU oven)
Cost Estimate and Schedule for Production

- Components (including TTCrq mezzanine).............. $530 \times 70 = $37,100
- Services (PCB & front panel fabrication, assembly).... $500 \times 70 = $35,000

Total.................. $72,100

Make schematic/layout changes and build 3 sample boards... Sept - Nov 2004
Order all components .................................................. Sept - Nov 2004
Assemble/Test 3 sample boards .................................................. December 2004
Would like to test this sample with the production peripheral backplane and crate
If OK fabricate the rest 67 boards ................................. January 2005
Assemble and test 67 boards ............................................. Feb – June 2005