Evaluation of the RTL Synthesis Tools for FPGA/PLD Design

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**Xilinx: Foundation ISE**

**Design Entry:** VHDL, Verilog, schematic, ABEL  
**Synthesis:** Xilinx XST, Synopsys FPGA Express  
**Fitter:** Xilinx proprietary  
**Simulator:** ModelSim Xilinx Edition  
**Test Bencher:** HDL Bencher

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**Altera: Quartus and Max+Plus**

**Design Entry:** VHDL, Verilog, schematic, AHDL  
**Synthesis:** Altera proprietary  
**Fitter:** Altera PowerFitter  
**Simulator and Test Bencher:** Integrated (Altera)

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**Simplified FPGA design flow (integrated development system)**
Simplified FPGA design flow with a third party synthesis tool
RTL (Register Transfer Level) Synthesis program translates, along with user-defined constraints, an RTL model of hardware written in a HDL (VHDL or Verilog) into a gate-level netlist for place and route.

Typical Features:

- Language-sensitive editor with automatic syntax and synthesis checks for both Verilog and VHDL
- Proprietary timing-driven synthesis algorithms for logic optimization and technology mapping
- Block- and gate-level graphical results
- Tools for critical path analysis and retiming
- Industry standard outputs for P&R (EDIF)
- Support for virtually all PLD/FPGA vendors and families
- Seamless interface with the integrated systems (Xilinx, Altera etc)
Launch the software

Set up Files

Set Constraints

Set Options

Run Synthesis

Analyze Results

Source files

Fmax, i/o delays, attributes etc

Vendor-specific options

Compilation, optimization and mapping into vendor-specific technology

Block diagrams, schematics, tables

To Place and Route

Typical RTL Synthesis Design Flow
Most Popular Third Party PLD/FPGA RTL Synthesis Tools for PC (Windows)

- **FPGA Express (Synopsys).** Available at the Xilinx Foundation ISE integrated system in addition to Xilinx XST synthesis. Free companion to Altera Max+Plus and Quartus systems. Full version is available for evaluation (www.synopsys.com).

- **FPGA Compiler II (superset of FPGA Express) (Synopsys).** Available for evaluation (www.synopsys.com).

- **Leonardo Spectrum (Exemplar Logic, Mentor Graphics).** (Altera-only version is a free companion to Altera Max+Plus and Quartus systems. Available for downloading from Altera website.

- **Sinplify Pro (Synplicity).** 20-day free trial version is available for downloading from www.synplicity.com
The goal of evaluation:

1. Create a sample chip-independent hierarchical VHDL project

2. Run this project through the integrated development system (Altera or Xilinx) and get a results (performance and resource usage).

3. Run the same project through a third party synthesis (several tools), import the output EDIF file into vendor specific P&R tool (Altera or Xilinx) and get a results (performance and resource usage).

4. Compare results obtained in 1 and 2.
Sample Project

- Sorter “3 objects out of 18”
- Project consists of 7 vendor-independent VHDL design files
- Sorting is based on 4-bit patterns
- 72 data inputs, 1 clock input, 54 outputs, no PLL/DLL, no RAM/ROM/FIFO
Results of Synthesis and P&R (Altera Quartus II v.1.0)

- **Target device - Altera 20K60EFC324-1**
- **Both synthesis and P&R are optimized for speed**

<table>
<thead>
<tr>
<th></th>
<th>Quartus II v.1.0</th>
<th>Leonardo v.2001-1a28</th>
<th>FPGA Express 2000.11-FE3.5</th>
<th>Synplify Pro 6.2.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of LC used</td>
<td>1539/2560 (60%)</td>
<td>1430/2560 (55%)</td>
<td>1823/2560 (71%)</td>
<td>1442/2560 (56%)</td>
</tr>
<tr>
<td>Fmax after P&amp;R, MHz</td>
<td>39.86</td>
<td>44.87</td>
<td>40.42</td>
<td>48.87</td>
</tr>
</tbody>
</table>

* EDIF output was imported into Quartus II for P&R
Results of Synthesis and P&R (Altera Quartus II v.1.0)

- Target device - Altera 20K100CF324C7
- Both synthesis and P&R are optimized for speed

<table>
<thead>
<tr>
<th></th>
<th>Quartus II v.1.0</th>
<th>Leonardo v.2001-1a28</th>
<th>FPGA Express 2000.11-FE3.5</th>
<th>Synplify Pro 6.2.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of LC used</td>
<td>1539/4160 (36%)</td>
<td>1430/4160 (34%)</td>
<td>1823/4160 (43%)</td>
<td>1319/4160 (32%)</td>
</tr>
<tr>
<td>Fmax after P&amp;R, MHz</td>
<td>47.49</td>
<td>56.19</td>
<td>46.72</td>
<td>56.45</td>
</tr>
</tbody>
</table>

* EDIF output was imported into Quartus II for P&R
More investigation:

1. In a sample project the key VHDL design file (153 parallel comparisons) was replaced by functionally identical schematic file. All the rest settings and files in an Altera Quartus project were unchanged.

The overall design performance for the 20K60E PLD was up from 39.86MHz to 47.02MHz (~18%)! Resource usage is also better (55% vs 60%).

2. In a sample project the key VHDL design file (153 parallel comparisons) was replaced by functionally identical VHDL that uses an Altera \texttt{lpm\_compare} macrofunction. All the rest settings and files in a project were unchanged.

\begin{verbatim}
U1: lpm_compare
generic map (lpm_width => 4)
port map (dataa => INA, datab => INB, agb => OUTA(1));
\end{verbatim}

The overall design performance for the 20K60E PLD was up from 39.86MHz to 46.44MHz (~17%)! Resource usage is also better (56% vs 60%).

Conclusion: Quartus synthesis is more efficient for Altera-specific design sources including VHDL
Results of Synthesis and P&R (Xilinx Foundation ISE 3.3)

- **Target device** - Xilinx 2V250FG456-5
- **Synthesis is optimized for speed**

<table>
<thead>
<tr>
<th></th>
<th>ISE 3.3</th>
<th>ISE 3.3</th>
<th>Synplify Pro</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>XST</td>
<td>FPGA Express</td>
<td>6.2.4</td>
</tr>
<tr>
<td>Number of slices used</td>
<td>894/1536</td>
<td>(58%)</td>
<td></td>
</tr>
<tr>
<td>Fmax after P&amp;R, MHz</td>
<td>51.90</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* EDIF output was imported into Foundation ISE for P&R
Results of Synthesis and P&R (Xilinx WebPACK 3.3)

- Target device - Xilinx XC95288XV-7-TQ144
- Project - sorter “3 out of 6” (due to limited number of I/O)
- Synthesis is optimized for speed

<table>
<thead>
<tr>
<th></th>
<th>WebPACK XST</th>
<th>WebPACK XST</th>
<th>Synplify Pro 6.2.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of product terms used</td>
<td>838/1440</td>
<td>813/1440</td>
<td>713/1440</td>
</tr>
<tr>
<td></td>
<td>(58%)</td>
<td>(56%)</td>
<td>(49%)</td>
</tr>
<tr>
<td>Number of macrocells used</td>
<td>79/288</td>
<td>69/288</td>
<td>70/288</td>
</tr>
<tr>
<td></td>
<td>(27%)</td>
<td>(23%)</td>
<td>(24%)</td>
</tr>
<tr>
<td>Fmax after P&amp;R, MHz</td>
<td>33.40</td>
<td>33.70</td>
<td>42.10</td>
</tr>
</tbody>
</table>

* Schematic source for comparisons
** EDIF output was imported into WebPACK for P&R

CONCLUSION:
1. Xilinx XST synthesis is more efficient for Xilinx-specific than Xilinx-independent sources
2. Synplify Pro synthesis is more efficient than Xilinx XST
Results of Synthesis and P&R (Xilinx Foundation ISE 3.3)

- Target device - Xilinx V300EBG352-8
- Synthesis is optimized for speed

<table>
<thead>
<tr>
<th>Software</th>
<th>Number of slices used</th>
<th>Fmax after P&amp;R, MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISE 3.3 XST</td>
<td>904/3072 (29%)</td>
<td>41.76</td>
</tr>
<tr>
<td>ISE 3.3 FPGA Express</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Synplify Pro 6.2.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* EDIF output was imported into Foundation ISE for P&R
Why the Synplify Pro is more efficient than others?

Proprietary Behaviour Extracting Synthesis Technology (B.E.S.T.)
Algorithms based on:
• Conservation of Abstraction
• Integrated Module Generation
• Automatic Hierarchy Optimization
• Linear Compile Times

Integrated System for Simulation and Synthesis
Integrated Systems for Simulation and Synthesis

FPGA Advantage (Mentor Graphics). May 2001

- HDL Designer Series (Mentor) - design entry and management
- ModelSim (Model Technology) - simulation
- Leonardo Spectrum (Exemplar, Mentor Graphics) - synthesis


Active-HDL with Synplify (Aldec). August 2001

- Active-HDL - design entry and simulation
- Synplify (Synplicity) - synthesis
Conclusion

• Third party RTL synthesis tools may improve the overall design performance and resource usage for some projects up to 10..20% without changes in an original HDL code or/and P&R options.

• Synplify Pro (Synplicity) seems to be the most powerful PLD/FPGA third party RTL synthesis tool for PC (Windows). Available for free 20-day trial. Available on University program from Synplicity ($495 for three years, one node locked or 1-100 floating licenses).

• Integrated third party system comprising both simulation and synthesis could be the best companion tool for a vendor-specific development system, especially Xilinx Foundation ISE.